put voltage by simply waiting the right amount of time ($t=\log_2(V/V_{IN})T$) after starting the negative discharge. The divergent exponential and the negative time constant are the core concepts of the circuit in **Figure 2**.

You can program the amplifier's gain with a PWM (pulse-width-modulation) signal from a microcontroller or another circuit. When the PWM signal goes to logic zero, sample-and-hold capacitor C_1 charges to V_{IN}. When the PWM signal cycles to logic one, op amp A_1 drives the R_1C_1 positive-feedback loop, creating a negative time constant. The resulting divergent exponential rise of C_1's charge continues as long as the PWM signal remains at logic one. That situation creates a net voltage gain of:

$$V_{OUT}(t)=V_{IN}2^{(t/10\ \mu sec+0.5)}.$$

THE NEAR-UBIQUITY OF PROGRAMMABLE-TIMER/COUNTER HARDWARE MAKES IT EASY TO DIGITALLY GENERATE A HIGHLY REPEATABLE PWM-CONTROL SIGNAL.

Thus, gain $=2^{(t/10\ \mu sec+0.5)}$ and log(gain) $=3+0.6$ dB/μsec. At the end of the amplification cycle, when PWM returns to logic zero, amplifier A_2 captures and holds the amplified input voltage.

The logarithmic relationship between gain and timing provides excellent gain resolution even when a PWM signal has just 8 bits of resolution and its programmable gain has a range greater than 0.2 dB/LSB step. (To view the log and linear plots of gain versus time using the amplify phase, go to the Web version of this Design Idea at www.edn.com/090319dia.)

The accuracy and repeatability of the timing of the exponential signal, the ADC sampling, the jitter, and the RC-time-constant stability all limit the amplifier's gain-programming accuracy. In **Figure 2**, 1 nsec of timing error, or jitter, produces 0.007% of gain-programming error. Fortunately, the near-ubiquity of programmable-timer/counter hardware in microcontrollers and data-acquisition systems usually makes it easy to digitally generate a highly repeatable PWM-control signal. EDN

Instrumentation amplifier compensates system offset from single supply

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Many integrated instrumentation amplifiers have architectures that permit offset compensation. The reference terminal's voltage, V_{REF}, adds in phase to the output to yield a gain of one. As a result, you can reset the output offset voltage by applying to the V_{REF} input a correction voltage of equal value but of opposite polarity. If the instrumentation amp operates from a dual-supply voltage, you can easily provide both positive- and negative-correction voltage. However, some instrumentation amps operate from a single supply—for example, in a battery-powered application—to amplify a signal source or a sensor that introduces a positive offset voltage. A sensor such as the AD590 from Analog Devices (www.analog.com), for example, produces an output current proportional to absolute temperature, and you should calibrate it at the lower reference temperature. In this case, the output swing of the instrumentation amp decreases, especially with high gain. To prevent this effect, you must apply a negative-correction voltage, which you generate from the positive power supply. In precision applications, the application of such a voltage may cause a problem.

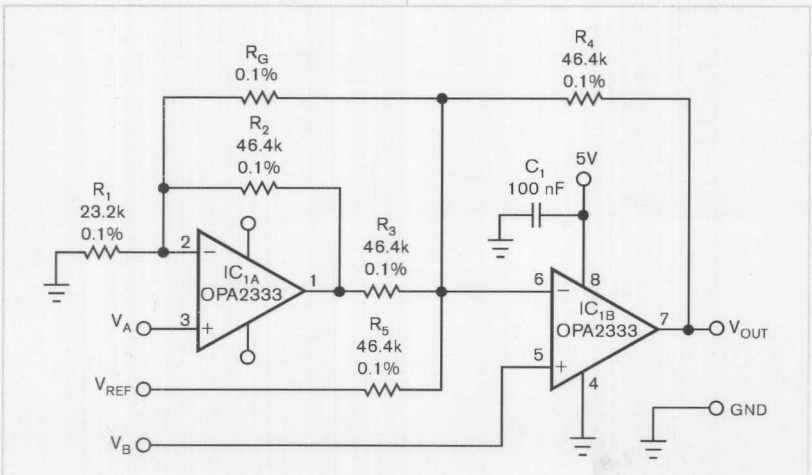

Figure 1 You can build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input.

This Design Idea shows you how to build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input. The circuit in **Figure 1** employs the dual high-precision OPA2333 op amp from Texas Instruments (www.ti.com). This op amp can

operate from a 1.8 to 5.5V supply and uses a proprietary autocalibration technique to simultaneously provide a maximum offset voltage of 10 μV and near-zero drift over time and temperature. It also offers high-impedance inputs that have a common-mode range 100 mV beyond the supply rails and rail-to-rail output that swings within 50 mV of the rails. Applying the superposition of the effects to the circuit in **Figure 1** yields the following **equation**:

$$V_O = V_B\left[\left(1+\frac{R_4}{R_3\|R_5\|R_G}\right)+\left(\frac{R_4}{R_3}\right)\left(\frac{R_2}{R_G}\right)\right]-V_A\left[\left(1+\frac{R_2}{R_1\|R_G}\right)\left(\frac{R_4}{R_3}\right)+\left(\frac{R_4}{R_G}\right)\right]-V_{REF}\left(\frac{R_4}{R_5}\right).$$

To achieve equal gain for both the V_B and the V_A inputs, resistors R_2, R_3, R_4, and R_5 must have equal values that are double the value of R_1. Using the resistor values in **Figure 1**, you obtain the following simplified **equation**:

$$V_O = \left(3+\frac{92.8\ k\Omega}{R_G}\right)(V_B-V_A)-V_{REF}.$$

The amplifier's differential gain is $3+(92.8\ k\Omega/R_G)$, and the reference voltage is added, inverted together with the output signal. Resistor R_G sets the gain, and, if you do not connect R_G, the gain assumes the minimum value, which is three; decreasing the value of R_G to 93Ω increases the gain to 1000.

The V_{REF} input requires a low-impedance connection to preserve a good CMRR (common-mode-rejection ratio); otherwise, you can use an op-amp buffer for better CMRR, which depends mainly on resistor-ratio matching. In this implementation, to preserve an acceptable CMRR, you must use precision film resistors. Analyzing the circuit, you can calculate the worst-case CMRR at low frequency. With R_2, R_3, R_4, and R_5 all of equal value and double that of R_1 and with all the resistors having equal tolerance, you obtain:

$$CMRR = \frac{3+\frac{2R}{R_G}}{6\left(\frac{\Delta R}{R}\right)},$$

where ΔR/R is the resistor's tolerance. If the tolerance is 0.1% and with the minimum differential gain, which is three, you obtain a CMRR of at least 54 dB. With a differential gain of 100, you obtain a CMRR of at least 84 dB.

The V_{REF} input can reduce the system offset to the lower output-swing limit but does not reset it completely because, in that case, the output voltage would be unable to reach the single-supply ground. If you want instead to reset the output offset, you can subtract this value using an ADC with differential inputs (**Reference 1**). EDN

REFERENCE

Bruno, Luca, "Circuit compensates system offset of a load-cell-based balance," *EDN*, Aug 16, 2007, pg 71, www.edn.com/article/CA6466208.